

SUBSTITUTE SPECIFICATION

TITLE OF THE INVENTION

SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device, and, more specifically, the invention relates to a technique which is effective for use in a multi-chip module in which plural semiconductor chips are mounted and 5 assembled on a common wiring substrate.

A multi-chip module in which plural LSI chips, such as a microprocessor and a memory are mounted on a common wiring substrate to build up a small computer system (for example, refer to Patent Document 1) has achieved widespread use in recent years.

10 In the multi-chip module technique, in which a printed substrate patterned in advance or a ceramic substrate as a common wiring substrate is used, plural bare LSI chips are disposed on this common wiring substrate, and pad electrodes of the LSI chips are bonded to patterns (conductive layers) on the wiring substrate by wire bonding, using the flip chip method, or the like, 15 thus packaging a computer system. The plural bare LSI chips can be disposed two-dimensionally in a plane, or they can be stacked up. As an example in which plural bare LSI chips are stacked up, a module can be mentioned in which an SRAM (Static Random Access Memory), is mounted so as to overlie a mobile system LSI, so that the need for a large capacity SRAM 20 is eliminated.

There is a well-known technique that appropriately converts the level

of a signal outputted from a signal output circuit without using external components, such as pull-up resistors, and transmits the converted signal to an external circuit driven by a voltage that is different from the voltage of the signal output circuit. In this case, on the final output stage of an LSI driven by 5 the driving power supply voltage of 5 volts, except for the final output stage, there are laid out inverter gates supplied with a driving power supply voltage that is independent from the above-mentioned driving power supply voltage. The output signal of the LSI is supplied to a power supply input terminal of the inverter gates, and the driving power supply voltage of the LSI is connected by 10 way of the power supply lines (for example, refer to Patent Document 2).

[Patent Document 1]

Japanese Unexamined Patent Publication No. Hei 9(1997)-331016

[Patent Document 2]

Japanese Unexamined Patent Publication No. Hei 11(1999)-41089

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SUMMARY OF THE INVENTION

In contrast to a single chip microprocessor of the type used for mobile equipment, that incorporates a large capacity SRAM, in the multi-chip module in which a universal SRAM of low power consumption is mounted to overlie the 20 microprocessor for the mobile equipment, with the large capacity SRAM being eliminated, each chip has two kinds of voltages, including a core voltage and an interface voltage. Therefore, when exchanging signals between the microprocessor and the external SRAM, the multi-chip module executes a level shifting of the signals, each individually in the I/O of the microprocessor 25 and in the I/O of the SRAM chip, to consequently obstruct speeding up memory accesses, as discovered by the inventor of this application.

The present invention has been made in view of the above-described technical problems, and an object of the invention is to provide a technique that makes it possible to speed up memory accesses in a semiconductor device.

5 The foregoing and other objects and novel features of the invention will become apparent from the following description and the appended drawings.

Typical aspects the present invention will be briefly described below.

According to one aspect of the invention, a semiconductor device includes a microprocessor and a semiconductor memory. Here, the
10 microprocessor includes an input/output buffer for the system side that is capable of exchanging signals with the outside when supplied with a power supply voltage. The semiconductor memory includes an internal power supply circuit that takes in the power supply voltage as a reference voltage, and generates an internal power supply voltage which is substantially equal to
15 the power supply voltage. The semiconductor memory also includes an input/output buffer for the memory side that is capable of exchanging signals with the input/output buffer for the system side when supplied with the internal power supply voltage.

In this arrangement, the power supply voltage for the microprocessor
20 supplied to the semiconductor memory is taken as a reference voltage, and the internal power supply voltage generated on the basis of the reference voltage is supplied to the input/output buffer for the memory side, which makes it possible to match the signal level of the input/output buffer for the memory side with that of an input/output buffer for the system side. This eliminates the
25 need for level shifting on the microprocessor side, which makes it possible to attain a high-speed access to the semiconductor memory from the

microprocessor.

Here, the semiconductor memory may include a dedicated external terminal for taking in the power supply voltage as a reference voltage. Further, the microprocessor may include internal circuits that are put in 5 operation when supplied with the power supply voltage. In order to simply configure the internal power supply circuit, it is preferred to include a differential circuit, that compares the power supply voltage taken in and an output voltage of the internal power supply circuit, and a voltage output circuit, that determines a level of the internal power supply voltage on the basis of a 10 comparison result produced in the differential circuit.

The semiconductor memory may include a memory internal circuit that is put in operation when supplied with a second internal power supply voltage of a higher level than the internal power supply voltage; and, the input/output buffer for the memory side may include a level shifting circuit that is capable of 15 shifting a signal level of the internal power supply voltage into a signal level of the second internal power supply voltage.

The semiconductor memory may include a step-down circuit that generates a third internal power supply voltage of a lower level than the internal power supply voltage, and a memory internal circuit that is put in 20 operation when supplied with the third internal power supply voltage; and, the input/output buffer for the memory side may include a level shifting circuit that is capable of shifting a signal level of the third internal power supply voltage into a signal level of the internal power supply voltage.

According to another aspect of the invention, the microprocessor 25 includes an internal core power supply circuit that steps down a power supply voltage that is externally supplied to thereby generate an internal core power

supply voltage, and an input/output buffer for the system side that is capable of exchanging signals with the outside when supplied with the internal core power supply voltage. The semiconductor memory includes an internal power supply circuit that takes in the internal core power supply voltage as a reference voltage, and generates an internal power supply voltage which is substantially equal to the internal core power supply voltage; and, an input/output buffer for the memory side that is capable of exchanging signals with the input/output buffer for the system side when supplied with the internal power supply voltage.

5 When the semiconductor memory is of a clock synchronous type, the microprocessor may include a clock driver that is capable of outputting a clock signal; and the semiconductor memory may include a clock buffer that takes in the clock signal outputted through the clock driver in the microprocessor, and a logic circuit that operates synchronously with the clock signal taken in through

10 the clock buffer.

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the clock buffer.

The microprocessor and the semiconductor memory may each be formed in separate chips, and these chips may be packaged integrally in a resin mold.

20 BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic circuit diagram showing the major part of a multi-chip module representing an example of the semiconductor device of the invention;

Fig. 2 is a perspective view of the multi-chip module schematically represented in Fig. 1;

Fig. 3 is a block diagram of the microprocessor included in the

multi-chip module;

Fig. 4 is a block diagram of the SRAM included in the multi-chip module;

Fig. 5 is a schematic circuit diagram showing a modification of the 5 SRAM in the multi-chip module;

Fig. 6 is a perspective view of another embodiment of the multi-chip module representing an example of the semiconductor device of the invention;

Fig. 7 is a schematic circuit diagram showing a major part of the multi-chip module illustrated in Fig. 6; and

10 Fig. 8 is a schematic circuit diagram showing a major part of the multi-chip module.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 2 illustrates a multi-chip module which represents an example of a 15 semiconductor device relating to the present invention. The multi-chip module 1 illustrated in Fig. 1 includes a microprocessor 10 in the form of a system LSI, an SRAM (Static Random Access Memory) 20 that is capable of being accessed by the microprocessor 10, and a substrate 30 on which the former two elements are mounted, although the invention is not specifically so 20 restricted; and this structure is integrally packaged by resin molding. The microprocessor 10, SRAM 20, and substrate 30 each have bonding pads 11-1 to 11-n, 21-1 to 21-n, 31-1 to 31-2, respectively, formed thereon. By bonding these pads with bonding wires, signal exchange and power supply between 25 and to the respective elements become possible. The SRAM 20 is used to provide work areas and the like in the processing performed by the microprocessor 10. Accordingly, the microprocessor 10 does not contain an

SRAM to provide work areas and the like.

Fig. 3 is a block diagram of the microprocessor 10. As shown in Fig. 3, the microprocessor 10 includes a central processing unit (CPU) 101, a read only memory (ROM) 102, an input/output buffer 103 for the system side, a 5 direct memory access controller (DMAC) 104, and a bus state controller (BSC) 105, although the invention is not specifically so restricted; and these components are formed on one semiconductor substrate, such as a single crystal silicon substrate, by means of a well-known method of manufacture of semiconductor integrated circuits. The CPU 101, ROM 102, input/output 10 buffer 103, DMAC 104, and BSC 105 are coupled by way of a bus 106 to permit an exchange of signals therebetween.

The ROM 102 holds the programs that are executed by the CPU 101. The input/output buffer 103 for the system side makes it possible to exchange various signals with the outside through the bonding pads, which will be 15 described in detail later. Especially, the CPU 101 is able to access the SRAM 20 through the input/output buffer 103. The DMAC 104 controls the DMA transfer of data between the memories (not illustrated) inside and outside the chip, and between integrated peripheral modules. The BSC 105 controls the bus state, for example, the insertion of a wait cycle.

20 Fig. 4 is a block diagram of the SRAM 20.

As shown in Fig. 4, the SRAM 20 includes a memory cell array 201, a row decoder 202, a controller 203, a column selection circuit 204, a column decoder 205, an input/output buffer 206 for the memory side, and an internal power supply circuit 207, although the invention not specifically so restricted; 25 and these components are formed on one semiconductor substrate such as a single crystal silicon substrate, by means of a well-known method of

manufacture of semiconductor integrated circuits.

The memory cell array 201 includes plural word lines, plural bit lines disposed to intersect the word lines, and plural static-type memory cells disposed on the intersecting points of the word lines and the bit lines. The 5 row decoder 202 decodes row address signals, and thereby generates a signal for driving one word line among the plural word lines to the selection level. The column selection circuit 204 includes plural column selection switches for connecting the plural bit lines selectively to a common line. The column decoder 205 decodes column address signals, and thereby generates a 10 driving signal for the column selection switches. The input/output buffer 206 for the memory side includes an output circuit that externally outputs data of the common line, and an input circuit that fetches write data to the memory cell array 201 from the outside. The controller 203 generates timing signals for operating the related parts according to control signals supplied from the 15 outside. The internal power supply circuit 207 takes in the power supply voltage used in the microprocessor 10 as a reference voltage, and generates an internal power supply voltage VDD'. The internal power supply voltage VDD' is supplied mainly to the input/output buffer 206 for the memory side.

Fig. 1 illustrates a major part of the microprocessor 10 and a major part 20 of the SRAM 20.

In the microprocessor 10, the bonding pads 11-1 and 11-2 are bonded respectively to the bonding pads 30-1 and 30-2 on the substrate 30, which make it possible to take in a high potential power supply voltage VCC and a 25 high potential power supply voltage VDD. The high potential power supply voltage VCC is set to 3.3 V, and the high potential power supply voltage VDD is set to 1.5 V, although the invention is not specifically so restricted. The high

potential power supply voltage VDD is supplied to the core parts in the microprocessor 10, such as the CPU 101, ROM 102, input/output buffer 103, DMAC 104, BSC 105, etc. Here, a low potential power supply voltage VSS (ground level) is defined as the Low level of the signals exchanged between 5 the CPU 101, ROM 102, input/output buffer 103, DMAC 104, and BSC 105; and the high potential power supply voltage VDD (1.5 V) is defined as the High level.

The plural bonding pads 11-3 to 11-n are bonded to the plural bonding pads 21-3 to 21-n in the SRAM 20 by wire bonding. The input/output buffer 10 103 includes plural input/output buffers 103-3 to 103-n corresponding to the plural bonding pads 11-3 to 11-n. The input/output buffer 103-3 as a representative example is configured as follows.

The output buffer is formed of a NAND gate 71, that attains the negative AND state in response to receipt of a logic of specific bits of the bus 15 106 and a write enabling signal WE; a p-channel MOS transistor 73, whose operation is controlled by an output signal from the NAND gate 71; an inverter 70 that inverts the logic state of the write enabling signal WE showing the validity of data being written into the SRAM 20; a NOR gate 72 that attains the negative OR state in response to receipt of an output signal from the inverter 20 70 and the logic of specific bits of the bus 106; and an n-channel MOS transistor 74, whose operation is controlled by an output signal from the NOR gate 72, whereby the logic state of specific bits of the bus 106 is transmitted to the bonding pad 11-3 within a period where the write enabling signal WE is asserted to the High level. The output buffer also includes a NAND gate 81 25 that attains the negative AND state in response to receipt of a logic state of the bonding pad 11-3 and a read enabling signal RE showing the validity of data

being read out from the SRAM 20; a p-channel MOS transistor 83, whose operation is controlled by an output signal from the NAND gate 81; an inverter 80 that inverts a logic state of the read enabling signal RE; a NOR gate 82 that attains the negative OR in response to receipt of an output signal from the inverter 80 and the logic state of the bonding pad 11-3; and an n-channel MOS transistor 84, whose operation is controlled by an output signal from the NOR gate 82, whereby the logic state of the bonding pad 11-3 is transmitted to the bus 106 within a period where the read enabling signal RE is asserted to the High level.

10 In the period where the read enabling signal RE is negated to the Low level, both of the MOS transistors 83 and 84 are turned OFF, whereby the output impedances thereof are turned to a high impedance relative to the bus 106. The input/output buffers 103-4 to 103-n corresponding to the other bonding pads 11-4 to 11-n are also configured in the same manner as the 15 above-described input/output buffer 103-3.

 In case of the address signals and the various control signals, these signals are outputted only from the microprocessor 10 to the SRAM 20, and they will not be taken in from the SRAM 20 to the microprocessor 10. Therefore, the microprocessor 10 does not require input buffers and 20 possesses only output buffers, in regard to the buffers corresponding to the terminals (pads) of the address signals and various control signals.

 According to the input/output buffer 103 for system side, as thus configured, while the write enabling signal WE is asserted to the High level, the signal of the bus 106 can be transmitted to the SRAM 20 through the bonding pads 11-3 to 11-n. While the read enabling signal RE is asserted to the High 25 level, the signal transmitted from the SRAM 20 can be taken in through the

bonding pads 11-3 to 11-n, and this signal can be transmitted to the bus 106.

In the SRAM 20, the bonding pads 21-1 and 21-2 are bonded, respectively, to the bonding pads 30-1 and 30-2 on the substrate 30, so that the high potential power supply voltage VCC and the high potential power supply voltage VDD can be taken in. The high potential power supply voltage VCC is supplied to the controller 203, row decoder 202, column decoder 205, and internal power supply circuit 207 and so forth. The high potential power supply voltage VDD is taken into the internal power supply circuit 207 as a reference voltage.

The internal power supply circuit 207 takes in the high potential power supply voltage VDD as a reference voltage Vref, which is transmitted through the bonding pad 21-2 (this high potential power supply voltage VDD is also supplied to the input/output buffer 103 for system side in the microprocessor 10), and it is used to generate the internal power supply voltage VDD'. Here, the potential level of the internal power supply voltage VDD' is made substantially equal to that of the high potential power supply voltage VDD. The internal power supply circuit 207 is configured as follows.

The internal power supply circuit 207 is provided with a capacitor 46 that removes the noise components contained in the high potential power supply voltage VDD that is transmitted through the bonding pad 21-2. The high potential power supply voltage VDD is transmitted to the gate electrode of an n-channel MOS transistor 42. An n-channel MOS transistor 41 is differentially coupled with the n-channel MOS transistor 42. The drain electrodes of the MOS transistors 41, 42 are connected to the load of a current mirror circuit configured with p-channel MOS transistors 44, 45, which are connected to the high potential power supply voltage VCC. The source

electrodes of the MOS transistors 41, 42 are connected to the low potential power supply voltage VSS through a constant current source 43. The drain electrode of the MOS transistor 42 supplies an output signal of the differential pair. The output signal of the differential pair is transmitted to the gate electrode of the p-channel MOS transistor 47. The source electrode of the p-channel MOS transistor 47 is connected to the high potential power supply voltage VCC, and the drain electrode of the p-channel MOS transistor 47 is connected to the low potential power supply voltage VSS through a resistor 48. The current flowing through the resistor 48 is controlled according to the output signal of the differential pair, whereby the level of the output voltage VDD' of the internal power supply circuit 207 is determined. In this sense, the series circuit of the p-channel MOS transistor 47 and the resistor 48 is referred to as an voltage output circuit. The output voltage VDD' of the internal power supply circuit 207 is transmitted to the gate electrode of the MOS transistor 41, whereby the differential pair of the MOS transistors 41, 42 produces a difference of the high potential power supply voltage VDD and the output voltage VDD' of the internal power supply circuit 207. Based on this difference, the current flowing through the resistor 48 is controlled by the MOS transistor 47, whereby the output voltage VDD' of the internal power supply circuit 207 is controlled so as to be substantially equal to the high potential power supply voltage VDD. The output voltage VDD' of the internal power supply circuit 207 is supplied to the input/output buffer 206 for the memory side.

The input/output buffer 206 for memory side includes plural input/output buffers 206-3 to 206-n corresponding to the plural bonding pads 21-3 to 21-n. The input/output buffer 206-3 as a representative example is

configured as follows.

The input/output buffer is formed of a NAND gate 51, that attains the negative AND state in response to receipt of an output signal OUT1 and an output enabling signal OE; a p-channel MOS transistor 53, whose operation is controlled by an output signal from the NAND gate 51; an inverter 50 that inverts the logic state of the output enabling signal OE; a NOR gate 52 that attains the negative OR state in response to an output signal from the inverter 50 and the output signal OUT1; and an n-channel MOS transistor 54, whose operation is controlled by an output signal from the NOR gate 52, whereby the output signal OUT1 is transmitted to the bonding pad 21-3 within a period where the output enabling signal OE is asserted to the High level. Although the high potential power supply voltage VCC is supplied to the NAND gate 51, inverter 50, and NOR gate 52, since the internal power supply voltage VDD' is supplied to the source electrode of the p-channel MOS transistor 53, the High level of the output signal from the input/output buffer 206-3 is equal to the level of the internal power supply voltage VDD', which is substantially equal to the level of the high potential power supply voltage VDD.

A NOR gate 61 attains the negative OR state in response to a signal of the bonding pad 21-3 and the write enabling signal WE, and a post-stage level shifting circuit converts the level of the output signal from the NOR gate 61 into that of the high potential power supply voltage VCC. The level shifting circuit is configured to include an inverter 60 that inverts the logic state of the output signal from the NOR gate 61, p-channel MOS transistors 58, 59, and n-channel MOS transistors 56, 57. The p-channel MOS transistor 58 and the n-channel MOS transistor 56 are connected in series, and the p-channel MOS transistor 59 and the n-channel MOS transistor 57 are connected in series.

The source electrodes of the p-channel MOS transistors 58, 59 are connected to the high potential power supply voltage VCC, and the source electrodes of the n-channel MOS transistors 56, 57 are connected to the low potential power supply voltage VSS. The series connection node of the p-channel MOS

5 transistor 58 and the n-channel MOS transistor 56 is connected to the gate electrode of the p-channel MOS transistor 59, and it is also connected to an internal circuit contained in the SRAM 20. The series connection node of the p-channel MOS transistor 59 and the n-channel MOS transistor 57 is connected to the gate electrode of the p-channel MOS transistor 58. The

10 output signal from the NOR gate 61 is transmitted to the gate electrode of the n-channel MOS transistor 57 and also to the gate electrode of the n-channel MOS transistor 56 by way of the inverter 60. Although the internal power supply voltage VDD' is supplied to the NOR gate 61 or the inverter 60 as a power supply, since the high potential power supply voltage VCC is supplied to

15 the source electrodes of the p-channel MOS transistors 58, 59, the signal of the internal power supply voltage VDD' level is converted into the signal IN1 of the high potential power supply voltage VCC level, and then the level-converted signal is transmitted to the internal circuits.

The other input/output buffers 206-4 to 206-n are configured in the

20 same manner.

Here, in regard to the various types of control signals, such as the output enabling signal OE and the write enabling signal WE, and the address signals, the microprocessor 10 transmits such signals to the SRAM 20; however, in contrast, the SRAM 20 will not transmit such signals to the

25 microprocessor 10. Therefore, the SRAM 20 does not require output buffers and possesses only input buffers, with regard to the buffers corresponding to

the terminals (pads) that take in the various control signals, such as the output enabling signal OE and the write enabling signal WE, and the address signals.

The above-described embodiment exhibits the following functions and effects.

5 (1) The SRAM 20 takes in the high potential power supply voltage VDD, which is used as the core voltage (VDD) of the microprocessor 10, as a reference voltage, and it generates the internal power supply voltage VDD' that is substantially equal to the high potential power supply voltage VDD; and the internal power supply voltage VDD' is supplied to the input/output buffer 206
10 for the memory side as an operational power supply voltage. Therefore, in the input/output buffer 103 for the system side of the microprocessor 10, level shifting becomes unnecessary, which makes it possible to couple the input/output buffer 206 for the memory side with the bus 106 of the microprocessor 10 through the input/output buffer 103 for the system side
15 using a comparably simple configuration. Accordingly, the embodiment achieves a speed-up of the signals exchanged between the microprocessor 10 and the SRAM 20, compared to the conventional circuit in which both the microprocessor 10 and the SRAM 20 carry out a level shifting of the signals.

(2) Since the SRAM 20 generates an internal power supply voltage
20 VDD' which is substantially equal to the high potential power supply voltage VDD, using the core voltage (VDD) of the microprocessor 10 as a reference voltage, even if the core voltage (VDD) of the microprocessor 10 is changed, the interface level between the microprocessor 10 and the SRAM 20 will be matched; thus, the SRAM 20 possesses the flexibility to accommodate
25 diversification of the types of microprocessor 10.

Fig. 5 illustrates another circuit configuration of the SRAM 20, which

represents a modification of that shown in Fig. 1.

The SRAM 20 illustrated in Fig. 5 greatly differs from the one illustrated in Fig. 1 in the following points. That is, the modified SRAM 20 is provided with a step-down circuit 9 that steps down the high potential power supply voltage VCC to thereby generate an internal power supply voltage VDDi, and it is also provided with a level shifting circuit that shifts the signal level of the internal power supply voltage VDDi system into that of the internal power supply voltage VDD' system.

The internal power supply voltage VDDi is set to a lower voltage than the internal power supply voltage VDD'. When the internal power supply voltage VDD' is set to 1.5 V, the internal power supply voltage VDDi is set to 1.3 V, although the invention is not specifically so restricted. The internal circuits of the SRAM 20, such as the row decoder 202, controller 203, column selection circuit 204, and column decoder 205 and so forth, become operational with the supply of the internal power supply voltage VDDi.

The input/output buffer 206 for the memory side includes plural input/output buffers 206-3 to 206-n corresponding to the plural bonding pads 21-3 to 21-n. The input/output buffer 206-3 as a representative example is configured as follows.

The input/output buffer 206-3 illustrated in Fig. 5 greatly differs from the one illustrated in Fig. 1 in the following points. That is, the former is provided with a level shifting circuit 91 that shifts the signal level of the output signal OUT1 into that of the internal power supply voltage VDD' system, and a level shifting circuit 92 that shifts the signal level of the output enabling signal OE into that of the internal power supply voltage VDD' system. The level shifting circuit 91 is configured to include an inverter 915 that inverts the logic

state of the output signal OUT1, p-channel MOS transistors 911, 912, and n-channel MOS transistors 913, 914. The p-channel MOS transistor 911 and the n-channel MOS transistor 913 are connected in series, and the p-channel MOS transistor 912 and the n-channel MOS transistor 914 are connected in series.

5 The source electrodes of the p-channel MOS transistors 911, 912 are connected to the internal power supply voltage VDD'. The source electrodes of the n-channel MOS transistors 913, 914 are connected to the low potential power supply voltage VSS. The series connection node of the p-channel MOS transistor 912 and the n-channel MOS transistor 914 is connected to the gate electrode of the p-channel MOS transistor 911, and it is also connected to the input terminal of the NAND gate 51 and the input terminal of the NOR gate 52. The series connection node of the p-channel MOS transistor 911 and the n-channel MOS transistor 913 is connected to the gate electrode of the p-channel MOS transistor 912. Thereby, the signal level of the output signal OUT1 is shifted from the signal level of the internal power supply voltage VDD' system into that of the internal power supply voltage VDD' system.

10 The level shifting circuit 92 is configured to include an inverter 925 that inverts the logic state of the output enabling signal OE, p-channel MOS transistors 921, 922, and n-channel MOS transistors 923, 924. The p-channel MOS transistor 921 and the n-channel MOS transistor 923 are connected in series, and the p-channel MOS transistor 922 and the n-channel MOS transistor 924 are connected in series. The source electrodes of the p-channel MOS transistors 921, 922 are connected to the internal power supply voltage VDD'. The source electrodes of the n-channel MOS transistors 923, 924 are connected to the low potential power supply voltage

VSS. The series connection node of the p-channel MOS transistor 922 and the n-channel MOS transistor 924 is connected to the gate electrode of the p-channel MOS transistor 921, and it is also connected to the input terminal of the NAND gate 51. The series connection node of the p-channel MOS 5 transistor 921 and the n-channel MOS transistor 923 is connected to the gate electrode of the p-channel MOS transistor 922, and it is also connected to the input terminal of the NOR gate 52. Thereby, the signal level of the output enabling signal OE is shifted from the signal level of the internal power supply voltage VDDi system into that of the internal power supply voltage VDD' 10 system.

As mentioned in the above case, when the internal power supply voltage VDDi, that is supplied to the internal circuits of the SRAM 20, is set to a lower level than the internal power supply voltage VDD', the input/output buffer 206 for the memory side only needs to contain the level shifting circuits 91, 92 15 to shift the signal level of the internal power supply voltage VDDi system into that of the internal power supply voltage VDD' system. This configuration will also exhibit the same function and effect as the one illustrated in Fig. 1.

Fig. 6 illustrates another configuration of the multi-chip module 1. The main difference between the multi-chip module 1 illustrated in Fig. 20 6 and the one illustrated in Fig. 2 lies in the fact that the bonding pad for the high potential power supply voltage VDD is eliminated from the substrate 30, and the bonding pad 11-2 on the microprocessor 10 is bonded to the bonding 25 pad 21-2 on the SRAM 20 by a bonding wire.

Fig. 7 illustrates a major part of the microprocessor 10 and the SRAM 20 illustrated in Fig. 6. The main difference between the microprocessor 10 25 illustrated in Fig. 7 and the one illustrated in Fig. 1 lies in the fact that the

microprocessor 10 contains an internal core power supply circuit 100 to generate the high potential power supply voltage VDD, which is obtained by stepping down the high potential power supply voltage VCC. The high potential power supply voltage VCC is set to 3.3 V, and the internal core power supply voltage VDD is set to 1.5 V, although the invention is not specifically so restricted. The internal core power supply voltage VDD is supplied to the internal cores (internal circuits), such as the CPU 101, ROM 102, DMAC 104, BSC 105, etc., as illustrated in Fig. 3, and the input/output buffer 103 for the system side.

The internal core power supply voltage VDD generated by internal core power supply circuit 100 is transmitted to the internal power supply circuit 207 as the reference voltage Vref through the bonding pad 11-2 on the microprocessor 10 and the bonding pad 21-2 on the SRAM 20. Thus, in the configuration illustrated in Fig. 1, the reference voltage Vref is transmitted through the bonding pad 30-2 on the substrate 30, however the configuration illustrated in Fig. 7 uses the voltage that the internal core power supply circuit 100 in the microprocessor 10 generates as the reference voltage Vref.

The other aspects of the configuration are the same as those illustrated in Fig. 1. The configuration using the core voltage (VDD) generated by the internal core power supply circuit 100 in the microprocessor 10 as the reference voltage Vref also exhibits the same function and effect as the one illustrated in Fig. 1.

When the core voltage (VDD) generated by the internal core power supply circuit 100 in the microprocessor 10 is transmitted to the SRAM 20, it is conceivable to directly supply the core voltage (VDD) to the input/output buffer 206 for the memory side. However, if the internal core power supply circuit

100 in the microprocessor 10 does not possess sufficient current capacity, there is a possibility that the core voltage (VDD) will decrease in voltage level undesirably. In contrast to this, as shown in Fig. 7, when the voltage generated by the internal core power supply circuit 100 in the microprocessor 5 10 is taken in as the reference voltage Vref, and based on that voltage, the internal power supply voltage VDD' is generated by the internal power supply circuit 207, the consumption of the reference voltage Vref itself is extremely insignificant; therefore, even if the internal core power supply circuit 100 in the microprocessor 10 does not possess sufficient current capacity, it is possible to 10 avoid a decrease in the voltage level of the core voltage (VDD) undesirably, which is advantageous.

The embodiments have been described with reference to specific configurations, however, the invention is not restricted to them, and it should be well understood that various changes and modifications are possible 15 without a departure from the spirit and scope of the invention.

For example, it is possible to supply a clock signal to the SRAM 20 from the microprocessor 10, and to operate the major part of the SRAM 20 synchronously with the clock signal. In this case, the SRAM 20 is made to synchronize with the clock. As shown in Fig. 8, for example, the 20 microprocessor 10 contains an internal clock generator 107 and a clock driver 108. The internal clock generator 107 generates an internal clock signal int. CLK on the basis of a clock signal taken in through a bonding pad 30-3 provided on the substrate 30 (refer to Fig. 2) and a bonding pad 11-CLK1 provided on the microprocessor 10. The internal clock signal int. CLK is 25 supplied to the internal circuits in the microprocessor 10, and it is also transmitted to the clock driver 108. The clock driver 108 drives an external

load on the basis of the transmitted internal clock signal int. CLK. Thereby, the internal clock signal int. CLK is transmitted to the internal circuits of the SRAM 20 through a bonding pad 11-CLK2 on the microprocessor 10 and a bonding pad 21-CLK1 on the SRAM 20.

5 The SRAM 20 possesses an input buffer 208 for the clock signal, and a D-type flip-flop 209 to operate synchronously with the clock signal which has been buffered by the input buffer 208. The signal being transmitted from the microprocessor 10 to the SRAM 20 is synchronized with the clock signal in the D-type flip-flop 209, and, thereafter, it is transmitted to an output buffer of the
10 input/output buffer 206 for the memory side, and then transmitted to the microprocessor 10 through the output buffer.

15 The input buffer 208 includes inverters 93, 94, 95, P-channel MOS transistors 98, 99, and n-channel MOS transistors 96, 97, etc. The p-channel MOS transistor 98 and the n-channel MOS transistor 96 are connected in series, and the p-channel MOS transistor 99 and the n-channel MOS transistor 97 are connected in series. The source electrodes of the p-channel MOS transistors 98, 99 are connected to the high potential power supply voltage VCC. The source electrodes of the n-channel MOS transistors 96, 97 are connected to the low potential power supply voltage VSS. The series
20 connection node of the p-channel MOS transistor 98 and the n-channel MOS transistor 96 is connected to the gate electrode of the p-channel MOS transistor 99, and it is also connected through the inverter 93 to the internal circuits and the D-type flip-flop 209.

25 The series connection node of the p-channel MOS transistor 99 and the n-channel MOS transistor 97 is connected to the gate electrode of the p-channel MOS transistor 98. The output signal from the inverter 94 is

transmitted to the gate electrode of the n-channel MOS transistor 97, and also to the gate electrode of the n-channel MOS transistor 96 by way of the inverter 95. Although the internal power supply voltage VDD' is supplied to the inverters 94, 95 as the power supply, since the high potential power supply 5 voltage VCC is supplied to the source electrodes of the p-channel MOS transistors 98, 99, the signal of the internal power supply voltage VDD' level is converted into the signal of the high potential power supply voltage VCC level, and then the level-converted signal is transmitted to the internal circuits and the D-type flip-flop 209. Thereby, the internal circuits and the D-type flip-flop 10 209 are operated in synchronism with the internal clock int. CLK being used in the microprocessor 10.

The invention has been described with reference to a configuration in which a microprocessor and an SRAM are stacked up, however, it is also applicable to a configuration in which a microprocessor and a semiconductor 15 memory, such as an SRAM, are arranged two-dimensionally in a plane.

The invention is applicable to a device on the condition that the device at least includes a microprocessor and a semiconductor memory that is capable of being accessed by the microprocessor.

The effect attained by the invention is as follows.
20 To supply a power supply voltage for a microprocessor into a semiconductor memory as a reference voltage, and to supply an internal power supply voltage generated on the basis of the reference voltage to an input/output buffer for the memory side, will make it possible to match the signal level of the input/output buffer for the memory side with that of an 25 input/output buffer for the system side; accordingly, level shifting on the microprocessor side becomes unnecessary, and a high-speed access to the

semiconductor memory from the microprocessor becomes possible.